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Field Effect Transistors Based on In Situ Fabricated Graphene Scaffold–ZrO_2 Nanofilms

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Ionic liquid-gated electric double layer transistors (EDLTs), bottom-gated field effect transistors (FETs), and vertical Schottky barrier transistors are fabricated by utilizing in situ prepared heterostrutural nanofilms. The nanofilms feature graphene scaffolds on top of high-k ZrO_2 dielectric, which allow transfer-free fabrication of various transistor devices. Both the ionic liquid-gated EDLT and bottom-gated FET feature p-type characteristic behaviors with notable I_{on}/I_{off} ratio and effective carrier modulation ability. Furthermore, the applicability of the layered structure is demonstrated in construction of vertical Schottky barrier transistors, and evident rectification behavior is revealed. With the capability to construct multilayer heterostructural nanofilms on various substrates and further optimizing the interfaces between these layers for targeted modulation, the presented electronic materials show potential application in graphene-based transistor fabrication.

Graphene-based devices have achieved considerable attention in recent years owing to the extraordinary electrical, mechanical, thermal, and optical properties of graphene-based materials.[1–6] Among them, field effect transistors (FETs) as the fundamental building units of modern electronic systems have been extensively studied using graphene for channel material fabrication.[7–10] Current chemical vapor deposition approaches using Cu[11] or Ni[12] as metal catalysts could be a preferred strategy for large-scale production of uniform graphene with large domain size. However, it usually requires an additional transfer process for fabricating graphene onto substrates, which is tedious and may affect the physical properties of graphene.[13] On the other hand, dielectric materials are of crucial importance in FETs because improved capacitance could be achieved by using gate dielectric layer for sufficient resistance (reduced gate leakage).[14,15] High-k dielectrics such as Al_2O_3,[16,17] HfO_2,[18,19] and ZrO_2[20,21] have been extensively used for the graphene-based FETs with nanometer regime, and emerged as potential alternate gate insulators replacing low-k SiO_2 in electronic devices. Therefore, for FETs, direct fabrication of graphene materials on top of high-k dielectrics, such as ZrO_2, without further transferring process will be of great importance.

Previously, we fabricated graphene scaffold–ZrO_2 nanofilms in situ on the SiO_2 substrates by spin coating and thermal annealing of a Zr-based metal–organic oligomer (**Figure 1**a).[22] The obtained nanofilm possesses heterostructure with ultrathin carbon layer formed on top of the ZrO_2 layer. The carbon layer shows a low sheet resistance of 17 kΩ per square, corresponding to 3197 S m^{-1} in electrical conductivity. In this study, we further investigated the detailed structural and electric characteristics of the obtained graphene scaffold–ZrO_2 nanofilms. Small angle X-ray reflectivity (XRR) confirms the heterostructure of the nanofilm, and a typical nanofilm is composed of ≈3.5 nm of carbon on top of ≈21.4 nm ZrO_2 layer. The resulting nanofilm on Si substrate shows a dielectric constant of ≈15.7, which is comparable to other high-k materials such as Y_2O_3 (≈15). The developed in situ strategy could be further utilized to build multilayer heterostructural films, such as graphene-ZrO_2/Al_2O_3 nanofilms on Si substrate, providing potential opportunities in building multilayer devices with various substrates. Further fabricating it into ionic liquid-gated electric double layer transistors (EDLTs) demonstrated the p-type channel characteristic of the graphene scaffold, with a current on-off ratio (I_{on}/I_{off}) of ≈2.1. With these desired structural and electric characteristics, we successfully integrated the graphene scaffold–ZrO_2 nanofilm into FETs with lateral architecture by applying either shadow masks or photolithography during electrode deposition, and these p-type FETs show notable I_{on}/I_{off} ratio.

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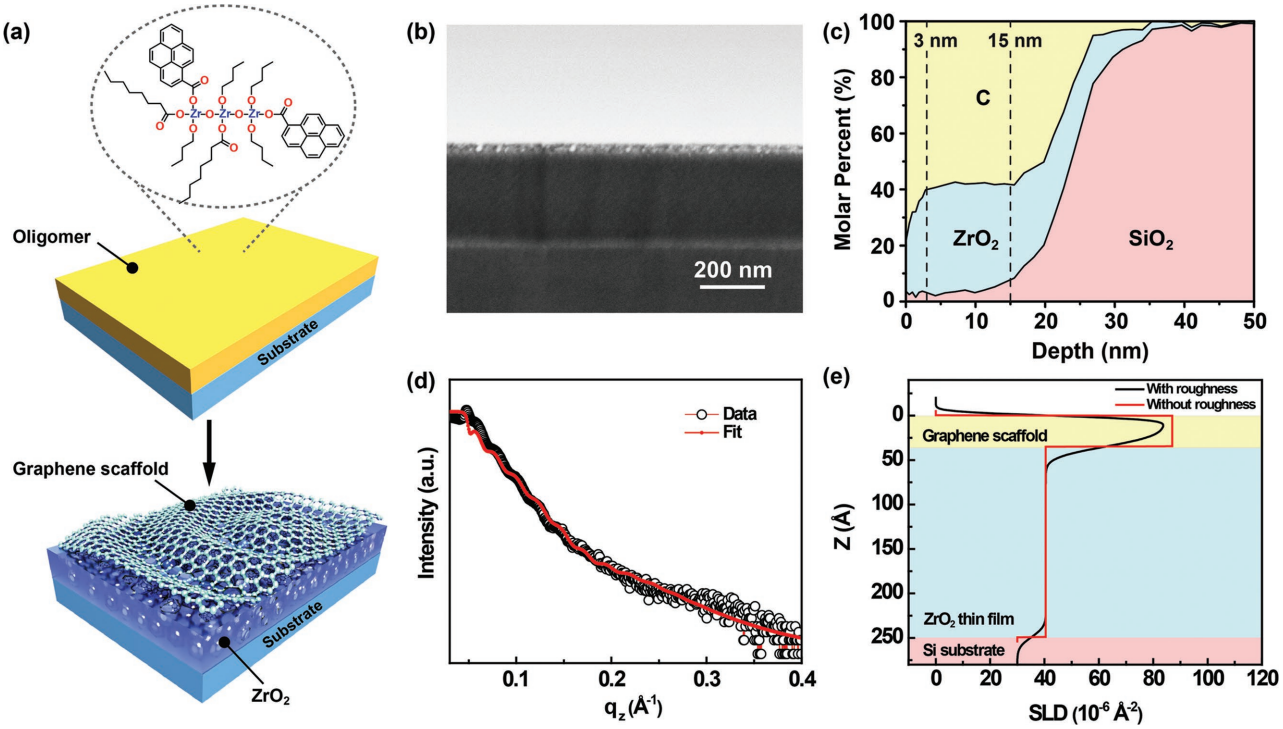

Figure 1. a) Schematic representation of the graphene scaffold–ZrO_2 nanofilm fabricated on the SiO_2/Si substrate from a Zr-based metal–organic oligomer. b) Cross-section SEM image of the graphene scaffold–ZrO_2 nanofilm on SiO_2/Si substrate. c) XPS depth profile of the nanofilm on SiO_2/Si substrate. The molar percent of C, ZrO_2, and SiO_2 was calculated based on the atomic percent of C, Zr, and Si. d) XRR measurement of the heterostructural nanofilm obtained at 900 °C for 20 min. e) SLD profile of the graphene scaffold–ZrO_2 nanofilm with (black) and without (red) roughness.

Furthermore, the heterojunction in the graphene scaffold–ZrO_2 nanofilm was investigated by fabricating it into Schottky barrier transistors, which shows rectification behavior. Overall, the in situ fabrication of graphene scaffold–ZrO_2 nanofilm and the construction of FETs without further transferring process demonstrate the applicability of the presented strategy in future electronic device fabrication.

Specifically, for graphene scaffold–ZrO_2 nanofilms fabrication, the Zr(IV) carboxylate coordination oligomer was first prepared by $Zr(OBu)_4$ and various aromatic carboxylates via a sol-gel process (see the Experiment Section in the Supporting Information for more details). The precursor solution was then spin-coated on the SiO_2/Si substrates and annealed at 900–1000 °C with a controlled ramping program under the continuous flow of 5% H_2/N_2 gas mixture to form graphene scaffold–ZrO_2 nanofilms (Figure 1a).[22] Cross-section scanning electron microscopy (SEM) image (Figure 1b) clearly shows the uniform and continuous nanofilm on the SiO_2/Si substrate with an average thickness of ≈23.8 nm. The composition of the obtained nanofilm was previously investigated by depth profiling analysis by X-ray photoelectron spectroscopy (XPS) and summarized in Figure 1c. Carbon content up to 78.5% on the very top of the surface implies a carbon-pure or carbon-rich layer, which is supported by an intergrowth layer of ZrO_2 and carbon from ≈3 to 15 nm in depth.[22] The conductivity of the intergrowth layer is $>10^3$ kΩ per square after the carbon-pure or carbon-rich layer is removed by O_2 plasma experiment,[22] indicating that the carbon-ZrO_2 intergrowth layer is not conductive, thus avoiding conductive path for current leakage in potential devices. XRR measurements were performed to further determine the layered structure of the graphene scaffold–ZrO_2 nanofilm (Figure 1d). The XRR curve of the nanofilm annealed at 900 °C for 20 min clearly shows the oscillatory behavior (termed as Kiessig fringe) with the corresponding fit, indicating that the nanofilm was uniformly stacked on the Si substrate. The scattering length density (SLD) profile (SLD = $\rho_e r_e$, where ρ_e is the electron density, and r_e is the classical electron radius) illustrates the formation of the graphene scaffold–ZrO_2 nanofilm, which could be modeled as a two-layer structure with different electron densities (Figure 1e). An ultrathin carbon layer (SLD = 8.7×10^{-7} Å^{-2}) with a thickness of ≈3.5 nm in situ formed on the ZrO_2 layer (SLD = 4.0×10^{-7} Å^{-2}) with ≈21.4 nm in thickness was deduced (Table S1, Supporting Information). This fit produced a total thickness of the graphene scaffold–ZrO_2 nanofilm being ≈24.9 nm for this sample, which was essentially consistent with that obtained from the SEM. In addition, the nanofilm annealed at 1000 °C for 60 min shows similar two-layer structure, with SLD = 8.0×10^{-7} Å^{-2} for ultrathin carbon layer (≈2.5 nm) and SLD = 4.5×10^{-7} Å^{-2} for ZrO_2 layer (≈22.4 nm), respectively (Figure S1 and Table S2, Supporting Information).

To investigate the dielectric property of the obtained graphene scaffold–ZrO_2 nanofilm, metal-oxide-semiconductor (MOS) devices were used to study the capacitance–voltage profile. The MOS devices based on graphene scaffold–ZrO_2 were fabricated with circular Au electrodes (150 nm in thickness and 400 μm in diameter) deposited with shadow masks. The *C–V* plot is shown in Figure S2 in the Supporting Information. Based on the highest capacitance in the *C–V* curve (700 pF) and

the thickness of the nanofilm (24.9 nm), the dielectric constant of the prepared nanofilm is calculated to be ≈15.7, which is comparable to other high-k materials, such as Y_2O_3 (≈15), but smaller than the reported value of ZrO_2 (≈25). This could be ascribed to the intergrowth of ZrO_2 and carbon in the film, in which the low-k carbon (less than 3.0) incorporation results in a reduction of the integral dielectric constant of the nanofilm.[23] In addition, the grain boundary between the ZrO_2 nanoparticles within the layer may also lower down the dielectric constant. Nevertheless, the ZrO_2 layer in the nanofilm still can be functioned as the high-k material for FETs fabrication.

The simultaneous formation of top graphene scaffold and bottom dielectric ZrO_2 layer renders a good opportunity to fabricate electric devices with well-defined semiconductor/dielectric interface, without any transfer process, and even without any exposure to atmosphere.[24] Furthermore, the facile Zr-based oligomer spin coating and thermal annealing strategy we proposed provides a wide applicability for fabricating different multilayer heterostructural films for various devices applications. As a proof of concept, we fabricated graphene scaffold–ZrO_2/pure ZrO_2 multilayer film on the Si substrate by a two-step method. The pure ZrO_2 layer between the graphene scaffold–ZrO_2 nanofilm and the Si substrate was first formed by thermal annealing of the Zr-based oligomer precursor in air. This pure ZrO_2 layer was confirmed by SEM, which shows that the ZrO_2 nanoparticles are closely packed and uniformly cover the whole Si wafer (Figure S3, Supporting Information). The same oligomer precursor was then spin-coated again on the preformed ZrO_2 layer and annealed under 5% H_2/N_2 gas mixture to form the graphene scaffold–ZrO_2 nanofilm (see the Experiment section in the Supporting Information for more details). Similarly, graphene scaffold–ZrO_2/Al_2O_3 multilayer film can also be fabricated by this method, in which the Al_2O_3 layer with thickness of ≈30 nm was first deposited on the Si substrate by atomic layer deposition. The top graphene scaffold–ZrO_2 nanofilm was then fabricated on the Al_2O_3 layer using the same annealing protocol. Overall, the successful fabrication of multilayer heterostructural films based on the Zr-based metal–organic oligomer suggests that the oligomer solution is compatible with diverse substrates, affording the opportunities for more sophisticated device fabrication.

For a better understanding of the heterostructural nature and the dielectric property of the graphene scaffold-ZrO_2 nanofilm, we fabricated EDLTs to investigate the carrier transport characteristic of the graphene scaffold. It was suggested that the use of ionic liquids (ILs) as gate dielectrics in the EDLTs can apply high electric fields at the interface between IL and solid with high carrier densities.[25–27] In our study, the EDLTs were fabricated by using *N*,*N*-diethyl-*N*-(2-methoxyethyl)-*N*-methylammonium bis-trifluoromethanesulfonyl)-imide (DEME-TFSI) as IL with planar device configuration, in which Cr/Au (5/50 nm) source (S) and drain (D) electrodes were patterned into Hall bar geometry with coplanar metal gate electrode (G) (**Figure 2**a). A drop of IL covered both the graphene scaffold with channel length/width (L/W) of 9/40 µm and the gate electrode (see the Experiment Section in the Supporting Information for more details). When electric potential was applied on the gate electrode, the cations and anions in the IL moved oppositely towards charged electrodes, and an electric double layer consist of a layer of cations in the IL and a layer of accumulated charges

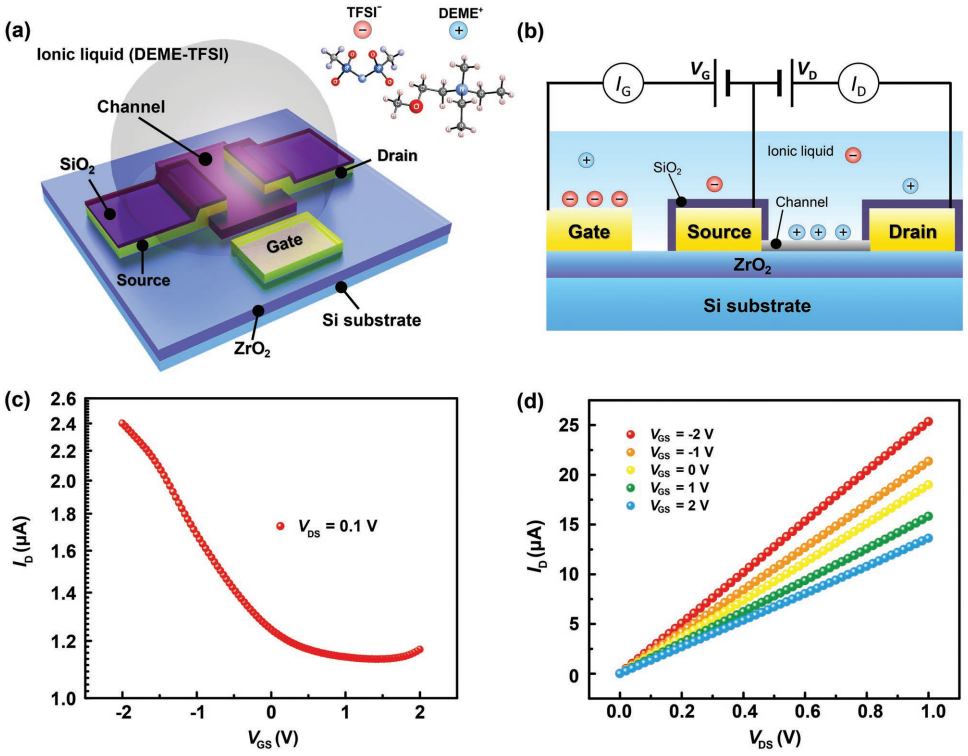

Figure 2. a,b) Schematic diagrams of an EDLT device with DEME-TFSI as ionic liquid. c) Transfer curve of EDLT device at V_{DS} = 0.1 V. d) Output curves of EDLT device with applied V_{GS} ranging from −2 to 2 V.

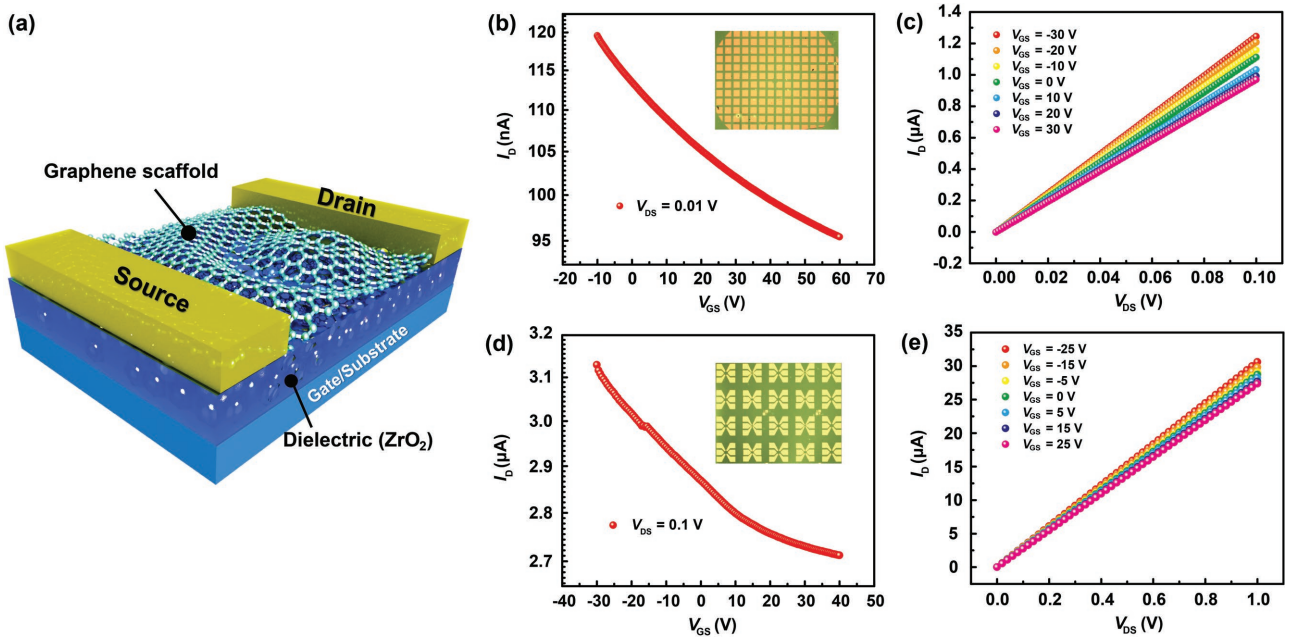

Figure 3. a) Schematic illustration of a bottom-gated FET device based on graphene scaffold–ZrO_2 nanofilm. b,c) Transfer and output characteristics of FETs with S/D electrodes deposited through shadow mask, with the image of the FETs shown as inset in (b). d,e) Transfer and output characteristics of FETs with S/D electrodes in Hall bar geometry, with the image of the FETs in Hall bar geometry shown as inset in (d).

in the graphene scaffold channel, was formed (Figure 2b). The obtained transfer curve (drain current I_D vs gate-source voltage V_{GS}, drain-source voltage V_{DS} = 0.1 V) in Figure 2c shows an obvious p-type characteristic that I_D gradually increases as V_{GS} reduces with a threshold of ≈0.5 V, indicating that negative V_{GS} promotes carriers (holes) accumulation in the channel. The maximum I_D with V_{DS} = 0.1 V at V_{GS} = −2 V is 2.4 μA, and the calculated I_{on}/I_{off} of the device is ≈2.1. In addition, the output curve (I_D vs V_{DS}) of the device (Figure 2d) shows nearly linear behavior without any saturation. This lack of current saturation is in common with many graphene-based metal-oxide-semiconductor field effect transistors (MOSFETs) due to the fact that graphene is a zero-band gap semiconductor.[2,28] The good linear regime of the device indicates that negligible energy barriers exist at the contact between Cr/Au electrodes and the graphene scaffold.[29] Moreover, the slope of I_D–V_{DS} curves increases clearly as V_{GS} reduces from 2 to −2 V at −1 V step, which is in accordance with the observation in the transfer curve, suggesting that the holes in the graphene scaffold channel can be effectively modulated by adjusting the gate voltages. Field effect mobility of ≈2.4 cm^2 $(V\ s)^{-1}$ in ambient condition is observed, which is lower compared to similar devices fabricated from high quality graphene (10^2–10^5 cm^2 $(V\ s)^{-1}$),[12,14] but still in the range of the typical carrier mobility values of ≈1–10 cm^2 $(V\ s)^{-1}$ for the reported reduced graphene oxide.[29,30] We conclude that the graphene scaffold fabricated in our work has defects, such as grain boundaries, lattice distortions, and small graphitic domain size, due to its intergrowth with ZrO_2 nanoparticles, and the defects limit the transport of carriers.

The effective carrier transport characteristic of the graphene scaffold proved its potential for FET devices by combining the graphene scaffold with the high-k ZrO_2. Cr/Au (5/50 nm) S/D electrodes were thermally deposited on the graphene scaffold–ZrO_2 nanofilm by using shadow masks to define the various channel lengths and widths (L/W of 40/85, 42/123, and 80/413 μm). The highly doped Si substrate served as gate electrode (**Figure 3**a). Of the many bottom-gated FET devices with varied channel lengths tested, all showed similar transfer characteristics regardless of the channel length. The transfer characteristic of the fabricated FET devices in Figure 3b shows the typical p-type behavior. The I_{on}/I_{off} in this device is ≈1.2, which is relatively smaller than that of the most reported MOSFET devices with large-area-graphene channels.[2] This can be attributed to the zero-band gap property of graphene and the intrinsic structural features of graphene scaffold–ZrO_2 nanofilm with intergrowth of ZrO_2 and carbon. Figure 3c shows the output characteristics of the FET device at different gate voltages from −30 to 30 V, in which all the I_D–V_{DS} curves exhibit linear shape, and the modulation of the carriers in the graphene scaffold channel by altering V_{GS} is achieved.

To check the possible effect of different processing technologies on the structure of the graphene scaffold and thus the electric performance of the devices, we also fabricated FET devices with S/D electrodes in multiterminal Hall bar geometry. Devices with different channel L/W of 40/17, 60/36, and 83/50 μm were tested. The devices also showed uniform transfer characteristics regardless of the channel length. The transfer characteristic of the Hall bar device in Figure 3d shows a similar p-type behavior, indicating that the majority accumulated carriers in the channel are holes. The output characteristics of the device at different gate voltages from −25 to 25 V (Figure 3e) show that device exhibits linear behavior and conductance increased slowly by reducing the gate voltage. It can be concluded that the graphene scaffold–ZrO_2 nanofilm could be applied to various processing technologies for device fabrication without losing the structural integrity.

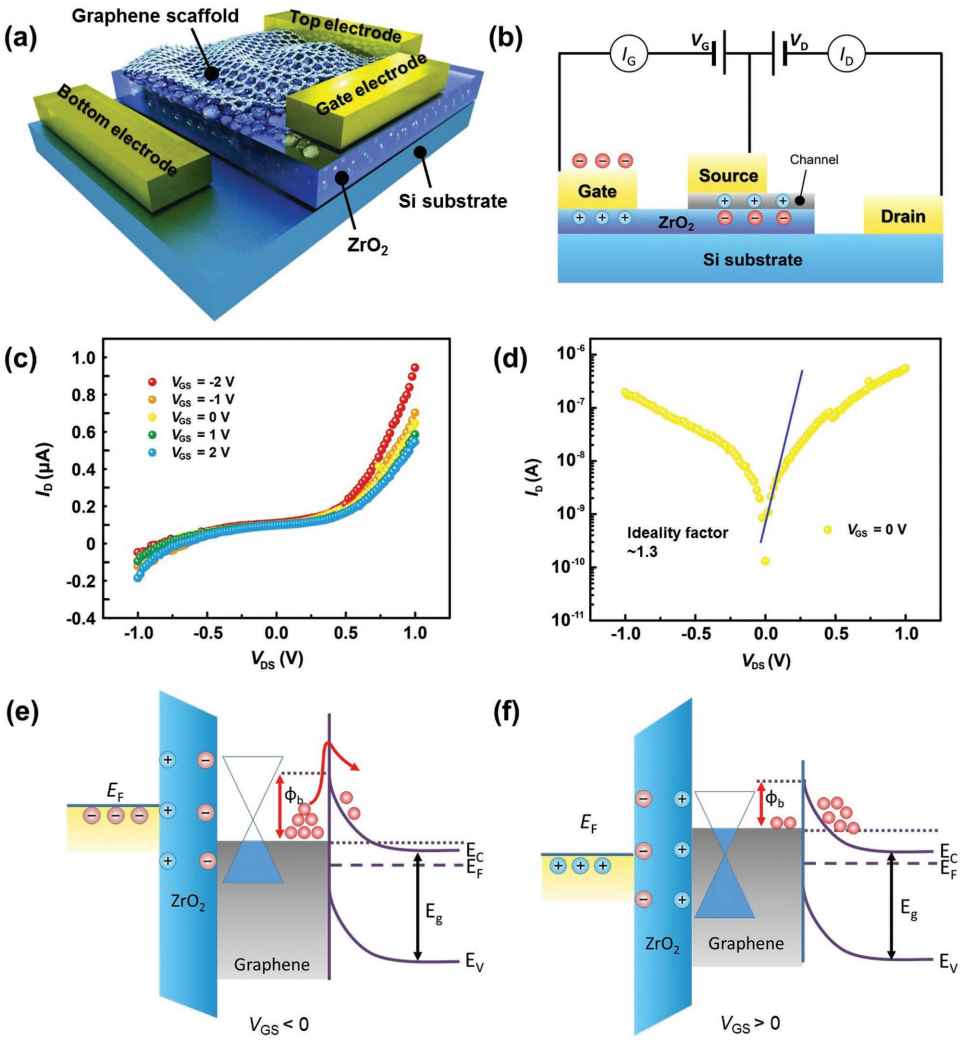

Figure 4. a,b) Schematics of the graphene scaffold–ZrO_2 heterojunction device. c) Output characteristics of the heterojunction device with V_{GS} ranging from –2 to 2 V. d) *I–V* curve of the heterojunction device with current I_D in logarithmic scale at V_{GS} = 0 V. The ideality factor was calculated by linear regression (blue line). e,f) Energy band diagrams of the heterojunction device in the on-state and off-state, respectively.

From the above electric performance analysis of the graphene scaffold–ZrO_2 based FET devices, we can see that the heterostructure serves as potential material for lateral FET fabrication, although the gate modulation ability of ZrO_2 dielectric is relatively weak at this stage. This is possibly caused by the intergrowth of ZrO_2 and carbon, which could lower the dielectric constant of the ZrO_2 layer. However, this intergrowth feature of the nanofilm along with the in situ fabrication process without further transferring renders it potential material for fabricating heterojunction devices. Therefore, we further fabricated Schottky barrier transistors based on the graphene scaffold–ZrO_2 nanofilm. Specifically, part of the graphene scaffold–ZrO_2 nanofilm was removed by photolithography technique, then the Cr/Au top and bottom electrodes were deposited on the areas with and without the nanofilm, respectively (**Figure 4**a,b). In addition, the gate electrode was deposited on the ZrO_2 layer directly after the graphene scaffold in this area was removed. The rectification behavior of the device is demonstrated in the output curves (Figure 4c) at various V_{GS}, in which I_D increased rapidly as V_{DS} surpassed the threshold voltage. A diode ideality factor of ≈1.3 for this device at V_{GS} = 0 V is observed with Schottky diode characteristic (Figure 4d). The transfer curve (Figure S4, Supporting Information) display typical p-type characteristic with an I_{on}/I_{off} of ≈1.6. The rectifying characteristic of the heterojunction device can be illustrated by the energy band diagram as shown in Figure 4e,f.[9] In the on-state (Figure 4e), when negative V_{GS} was applied on the gate electrode, holes in the graphene scaffold could be induced, which further increased the work function of graphene scaffold in our heterostructural material as well as the Schottky barrier height ϕ_b between graphene scaffold and ZrO_2 layer. Consequently, the reversed current across the Schottky barrier was reduced. On the other hand, in the off-state (Figure 4f), positive V_{GS} lowered down the Schottky barrier height ϕ_b, resulting in an increase in the reversed current.

In conclusion, diverse field effect transistors were fabricated with in situ formed graphene scaffold–ZrO_2 nanofilms from metal–organic oligomers. The in situ strategy allows

transfer-free preparation of graphene scaffold on ZrO_2 with a dielectric constant of 15.7 and a thickness of ≈25 nm, and it can be extended to the construction of mutltilayer heterostructural films on various substrates. By using IL as the gate dielectric, the graphene scaffold–ZrO_2 nanofilm based EDLT devices demonstrated the p-type characteristic of the graphene scaffold channel, with an I_{on}/I_{off} ratio of ≈2.1. With both the graphene scaffold layer and ZrO_2 layer, the nanofilm was further applied to fabricate p-type bottom-gated FET devices with notable I_{on}/I_{off} ratios using different processing techniques, confirming the material's adaptability in future device fabrication. Furthermore, the Schottky barrier transistors based on the graphene scaffold–ZrO_2 nanofilms present a rectification characteristic. Overall, the proposed approach via transfer-free graphene scaffold–ZrO_2 nanofilms for FETs demonstrates the feasibility of the heterostructures as building units for graphene transistors fabrication. With further optimization of the interface between the multilayer films, diverse graphene based transistors with high performance could be achieved.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Keywords

field effect transistors, graphene scaffold, high-k dielectrics, metal–organic oligomer, p-type characteristic

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